1. (original) A method, comprising:

receiving a clock signal defining a clock pulse period;

using the clock signal, generating at least one correction clock pulse, the correction clock pulse being temporally within a single clock period; and

using at least one correction clock pulse, latching values in plural data streams.

2. (original) The method of Claim 1, comprising generating at least 2N correction clock pulses for a single clock period, wherein N is an integer.

3. (original) The method of Claim 1, wherein at least two data streams have respective bits defining a temporally overlapping time period, and the method includes using at least one correction clock pulse in the overlapping time period to latch values in the streams.

4. (original) The method of Claim 1, wherein the clock signal is received from a phase locked loop and the correction clock pulses are generated by a voltage controlled oscillator (VCO).

5. (original) The method of Claim 4, comprising feeding back an output of the VCO to a phase detector receiving the clock signal.

6. (original) The method of Claim 1, comprising selecting at least one correction clock pulse for the using act using at least one selector element and at least one demultiplexer.

7. (original) A system for correcting jitter in data streams, comprising:

a correction clock module receiving a clock signal defining a clock pulse frequency and generating a correction clock signal having a frequency higher than the clock pulse frequency, the correction clock module latching values of at least two bits in respective data streams using at least one correction clock pulse within an overlapping period defined by the at least two bits.

8. (original) The system of Claim 7, wherein the correction clock module generates at least 2N correction clock pulses for a single clock signal period, wherein N is an integer.

9. (original) The system of Claim 7, wherein the clock signal is received from a phase locked loop and the correction clock pulses are generated by a voltage controlled oscillator (VCO).

[[11]] 10. (original) The system of Claim 9, wherein an output of the VCO is fed back to a phase detector receiving the clock signal.

[[12]] 11. (currently amended) The system of Claim [[11]] 10, comprising at least one selector element and at least one demultiplexer for selecting the correction clock pulse with which to latch bit values.

[[13]] 12. (currently amended) A jitter correction system comprising:

means for generating plural correction clock pulses for each clock pulse of a clock signal;

means for correlating at least a first correction clock pulse with at least two data bits received in respective parallel data streams; and

means for identifying values of the data bits at least in part using the first correction clock pulse, each correction clock pulse being composed of two signals, one being the opposite phase of the other.

[[14]] 13. (currently amended) The system of Claim [[13]] 12, wherein the means for generating includes at least one voltage controlled oscillator (VCO).

[[15]] 14. (currently amended) The system of Claim [[13]] 12, wherein the means for identifying includes at least one bus latch.

[[16]] 15. (currently amended) The system of Claim [[13]] 12, wherein the means for generating generates at least 2N correction clock pulses for a single clock period, wherein N is an integer.

[[17]] 16. (currently amended) The system of Claim [[13]] 12, wherein at least two data streams have respective bits defining a temporally overlapping time period, and the means for correlating correlates the first correction clock pulse by determining that the first correction clock pulse is in the overlapping time period.

[[18]] 17. (currently amended) The system of Claim [[14]] 13, comprising feeding back an output of the VCO to a phase detector receiving the clock signal.